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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,777	01/11/2002	Marc Chason	CMO1533I(72804)	8364

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,777	CHASON ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action is in response to Amdt. B, filed 8/8/03

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,335,571 to Capote et al. in view of U.S. Patent No. 5,258,648 to Lin.

Regarding claim 1, Capote discloses a method comprising: providing a semiconductor die (100, 10), and prior to placing the die on a printed wiring board (101, 20), disposing an underfill material (112, 37) on at least a portion of a second side thereof (figures 10-27).

Capote fails to disclose using an interposer with a semiconductor die attached to a first side thereof in place of using only a semiconductor die.

Lin discloses using an interposer (22) with a semiconductor die (12) attached to a first side thereof (figures 2 and 4; column 2, lines 39-65; column 3, lines 12-25; column 4, lines 49-68), rather than using only a semiconductor die, for attachment to a printed wiring board.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Capote, such that an interposer having at least one semiconductor die attached to a first side thereof is used in place of only a semiconductor die, as

taught by Lin. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an interposer with a semiconductor die in place of just a semiconductor die for bonding to a PWB, because Lin teaches that using an interposer allows for the thermal expansion compensation through use of an underfill disposed between the interposer and PWB, while still allowing a semiconductor die to be reworked or removed from the assembly (Lin, column 2, lines 39-65; column 3, line 55 – column 4, line 20). The combination of Capote and Lin allows a semiconductor die to be mounted on the PWB, burned in, tested, and removed if defective, without permanently attaching a defective die to the assembly (also see Lin, column 1, line 60 – column 2, line 21).

Regarding claims 4 and 5, Capote (as modified by Lin, supra) discloses the method steps of adding at least one interface electrode (30) to the second side of the interposer after disposing the underfill material (37; figures 19-21).

Regarding claim 6, Capote discloses disposing an underfill material on a portion of the second side thereof while simultaneously providing at least one aperture in the underfill material (column 10, lines 57-58; column 11, lines 18-21).

Regarding claim 7, Capote (as modified by Lin, supra) discloses adding at least one interface electrode (30) in the at least one aperture (figures 19-21).

Regarding claim 8, Capote discloses forming at least one aperture (38) in the underfill material (37), and adding at least one interface electrode (30) in the at least one aperture (figures 19-21).

Regarding claim 9, Capote discloses disposing an underfill including a plurality of material layers (column 4, lines 18 – 29; column 5, lines 10-36).

Regarding claims 10 and 11, Capote discloses exposing at least one of the material layers to low-temperature processing/drying (curing would inherently cause drying; column 12, lines 1-17; column 15, lines 1-7; column 5, line 32).

Regarding claim 12, Capote (as modified by Lin, supra) discloses removing at least a portion of the underfill material to expose at least a portion of at least one interface electrode (column 9, lines 59 – 62).

Regarding claim 13, Capote discloses using grinding or abrasion to expose the electrode (column 9, lines 59 – 62).

3. Claims 1-3, and 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Capote et al.

Regarding claims 1, 21, and 25, Lin discloses a method comprising: providing at least one interposer (22) having at least one semiconductor die (12) attached to a first side thereof (figures 1-5; column 5, lines 1-40); providing a printed wiring board (34); and attaching the interposer to the printed wiring board and underfilling the area between the interposer and PWB (column 5, lines 15-40).

Lin fails to disclose disposing a pre-form underfill on the second side of the interposer, with an interface electrode at least partially exposed through the underfilling material.

Capote teaches the use and advantages of a pre-form underfill (112, 37) with partially exposed electrodes (14, 30) disposed on the second side of a circuit element, which is then attached to a printed wiring board (column 2, line 1 – column 3, line 38; column 6, lines 19-29; figures 13, 17, 21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method/device of Lin such that a pre-form underfill is disposed on the interposer, as taught by Capote, rather than undergoing a process of underfilling. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to dispose an underfill material with partially exposed electrodes on the bottom of the interposer, because Capote teaches that conventional underfilling processes are generally disadvantageous, resulting in reduced production efficiency, increased production cost, increased production time, reduced reliability, and increased susceptibility to void formation or delamination (see Capote, column 2, line 48 – column 3, line 38). Capote then shows that the process of disposing an underfilling material on the component to be connected to the PWB, and then providing solder electrodes partially exposed through the underfilling, reduces or eliminates the problems with using a conventional underfilling method (see Capote, column 4, line 18 – column 6, line 30). Thus, it is well within the purview of a person having ordinary skill in the art to use the pre-formed underfill method taught by Capote in place of the conventional underfilling method, when attaching the interposer and chip of Lin on the PWB for the reasons listed supra.

Regarding claims 2, 3, 22, 26, and 28, Lin discloses that the interposer has solder balls (32) disposed on a second side thereof (figures 3 and 4; column 5, lines 3-14), the solder balls acting as a means for physically and electrically coupling the die to the PWB (figures 3 and 4).

Regarding claims 23 and 24, Lin fails to disclose further processing or heating the interposer on the PWB to at least partially harden the underfilling material.

Capote teaches heating of the interposer on the PWB to at least partially harden the underfilling material (column 9, lines 20-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Lin by heating the interposer on the PWB, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to heat the interposer/PWB assembly, because doing so cures the encapsulants, such that a continuous and voidless seal is formed between the PWB and chip component, as well as allow for the reflowing and connection of the solder joints of the chip component to the PWB (see Capote, column 9, lines 20-32). It is well within the purview of a person of ordinary skill to recognize that having a continuous seal between the components as well as fully reflowed solder joints improves the reliability of the assembly and provides protection for the assembly.

Regarding claim 27, Lin fails to disclose that the underfilling material comprises adherence means.

Capote teaches that the underfill comprises adherence means (column 8, lines 38-60; column 9, lines 20-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the underfilling material of Lin as modified by Capote, supra, comprises adherence means, as is further taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an underfilling material with adherence means, so that the chip component is reliably attached and affixed to the PWB, as is appreciated by one skilled in the art.

4. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Capote et al. as applied to claim 1 above, and further in view of European Patent Publication No. 0 475 022 A1 to Grube et al.

Regarding the claims, Lin fails to disclose providing a plurality of interposers disposed substantially co-planar to one another in a panel arrangement, disposing an underfill material on at least a portion of the second side of some of the plurality of interposers, and then singulating the interposers.

Grube discloses providing a plurality of interposers disposed substantially co-planar to one another in a panel, wherein at least some of the interposers each have at least one semiconductor die attached to one side thereof (see column 2, lines 32-58), disposing an attachment material on at least a portion of the second side of at least some of the plurality of interposers (adhesive is provided on the entire interposer sheet; see column 5, lines 23-39), and then singulating the interposers to provide singulated interposers (column 6, lines 5-18; figure 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Lin as modified by Capote, so that an interposer sheet is used when attaching chips and disposing underfill material as suggested by Grube. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an interposer sheet in place of a singulated interposer, because doing so allows for the processing steps involved with chip attachment, via patterning, and adhesive deposition to be formed for multiple interposers in a single step, rather than requiring separate manufacturing steps for each interposer (see Grube, column 2, lines 30-58).

5. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Capote et al. and further in view of Grigg, as applied to claim 18 above, and further in view of U.S. Patent No. 5,251,266 to Spigarelli et al.

Lin fails to disclose placing singulated interposers into a matrix tray carrier to facilitate subsequent placement of the singulated interposers on a printed wiring board.

Spigarelli discloses placing singulated IC devices in a matrix tray carrier (column 4, lines 1-4) to facilitate subsequent placement of the singulated devices on a printed wiring board (column 8, lines 38-45; column 13, lines 37-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Lin as modified by Capote and Grube, such that singulated interposers are placed into a matrix tray carrier, as taught by Spigarelli. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to place the singulated interposers into a carrier, so that the carrier features can be utilized to determine the position of each interposer, and thus allow for greater accuracy of placement onto a printed wiring board (Spigarelli, column 13, lines 37-68) as well as allow for automated pick and place bonding to a printed wiring board (Spigarelli, column 8, lines 38-45; column 13, lines 37-68).

Response to Arguments

6. Applicant's arguments filed 8/8/03 have been fully considered but they are not persuasive. The Applicant argues in item 6 of the response filed 8/8/03 that 'Capote does not teach providing a complete "underfilling" on either the die or the substrate alone - it is the final

combination that provides sufficient material to "fill" the available space.' This is not persuasive, because Capote does, in fact, teach an embodiment in which a complete underfilling is provided on the die (see figure 18). More importantly, however, the claim language does not require a 'complete underfilling' to be provided on the interposer, but rather only requires that an 'underfilling material' be provided on the interposer.

The applicant further argues that Capote teaches that 'interposers are to be used without an underfill material... In short, Capote teaches that interposers and underfill materials are different, alternative approaches to reliably securing a die to a substrate, and that the teachings regarding the use of a two-layer underfill material are solely directed to the latter and not to the former.'

This is not persuasive, because Capote does not in any way teach or suggest the means of attaching an interposer to a PWB, and only brings up an interposer as a generic prior art method. Capote is drawn specifically to a method of disposing an underfill material using a pre-formed underfill, rather than first attaching the chip component, and then underfilling. Capote further shows that the use of a pre-form underfill is specifically advantageous over a conventional underfilling process in terms of cost, labor, and reliability. Lin teaches that it is advantageous to attach a chip-interposer assembly to a PWB using an underfill, rather than attaching a bare chip using an underfill, because doing so allows for the specific advantage of being able to re-work the chip or replace a non-functioning chip with a functioning one. Thus, it is the examiner's opinion that it is well within the purview of a person having ordinary skill in the art to either substitute the chip-interposer assembly of Lin for the chip of Capote in the method of Capote, in order to provide the reworkability taught by Lin, or alternatively to substitute the pre-form

underfill of Capote for the conventional underfilling of Lin in the method of Lin, in order to achieve the improvements in cost, labor, and reliability taught by Capote. Since Capote does not really have any teachings at all pertaining to the use of an interposer, but rather merely mentions interposers as a general related-art means, it is the examiner's opinion that the combination of Capote and Lin does not constitute a method "contrary to the explicit teachings of Capote."

The remaining arguments filed 8/8/03 have been considered, but are moot based on the new grounds of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

Carl Whitehead Jr.
CARL WHITEHEAD, JR.
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